IN THE CLAIMS

1. (Currently Amended) A semiconductor structure comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer; and

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline silicon substrate;~~

~~an amorphous oxide material overlying the monocrystalline silicon substrate;~~

~~a monocrystalline perovskite oxide material overlying the amorphous oxide material;~~

~~a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material~~; and

a composite transistor comprising

a first transistor having first active regions formed at least in part in a silicon portion of the semiconductor structure,

a second transistor having second active regions formed at least in part in a monocrystalline compound semiconductor portion of the semiconductor structure, and

a mode control terminal for controlling the first transistor and the second transistor.

2. (Original) The semiconductor structure of claim 1 wherein the first transistor comprises a first field effect transistor having a monocrystalline silicon source region and a monocrystalline silicon drain region formed in the monocrystalline silicon substrate and the second transistor comprises a second field effect transistor having a monocrystalline compound semiconductor source region and a monocrystalline compound semiconductor drain region formed in the monocrystalline compound semiconductor material.

3.(Original) The semiconductor structure of claim 2 wherein the first transistor comprises a first gate associated with the monocrystalline silicon drain region and the monocrystalline silicon source region and coupled with the mode control terminal and the second transistor comprises a second gate associated with the monocrystalline compound semiconductor source region and the monocrystalline compound semiconductor drain region and coupled with the mode control terminal.

4.(Original) The semiconductor structure of claim 3 wherein the mode control terminal is configured to receive a signal to select one of a cut-off mode and a saturated mode for the first transistor and the second transistor.

5.(Original) The semiconductor structure of claim 2 further comprising:

a first multi-fingered gate separating the monocrystalline silicon source region and the monocrystalline silicon drain region; and

one or more switches for selectively actuating fingers of the first multi-fingered gate.

6.(Original) The semiconductor structure of claim 5 further comprising:

a second multi-fingered gate separating the monocrystalline compound semiconductor source region and the monocrystalline compound semiconductor drain region; and

one or more switches for selectively actuating fingers of the second multi-fingered gate.

7.(Original) The semiconductor structure of claim 6 further comprising:

a processor formed in the monocrystalline silicon substrate and coupled with the first multi-fingered gate and second multi-fingered gate to provide control signals to control selective actuation of the fingers of the first multi-fingered gate and second multi-fingered gate.

8.(Original) The semiconductor structure of claim 1 further comprising:

a signal input electrically coupled with a first active region of the first transistor and a first active region of the second transistor; and

a signal output electrically coupled with a second active region of the first transistor and a second active region of the second region.

9.(Original) The semiconductor structure of claim 1 further comprising

a silicon bipolar junction transistor formed at least in part in the monocrystalline silicon substrate; and

a heterojunction bipolar transistor formed at least in part in the monocrystalline compound semiconductor material.

10.(Original) The semiconductor structure of claim 9 wherein the silicon bipolar junction transistor and the heterojunction bipolar transistor each comprise a base contact electrically coupled with the mode control terminal.

11. (Currently Amended) A semiconductor structure comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer; and

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline silicon substrate;~~

~~an amorphous oxide material overlying the monocrystalline silicon substrate;~~

~~a monocrystalline perovskite oxide material overlying the amorphous oxide material;~~

~~a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material~~;

a silicon transistor formed at least in part in the monocrystalline silicon substrate;

a compound transistor formed at least in part in the monocrystalline compound semiconductor material;

a switch to selectively couple the silicon transistor and the compound transistor in response to a control signal; and

a control circuit configured to provide the control signal.

12. (Original) The semiconductor structure of claim 11 wherein the control circuit is formed at least in part of a silicon portion of the semiconductor structure.

13.(Original) The semiconductor structure of claim 11 further comprising:

a first input associated with a gate of the silicon transistor and configured to receive a first input signal;

a second input associated with a gate of the compound transistor and configured to receive a second input signal;

an output configured to provide a mixed signal when the switch receives a control signal associated with a mixer configuration; and

a matching network between source/drains of the silicon transistor and the compound transistor and the output.

14.(Original) The semiconductor structure of claim 11 further comprising:

a bias network to selectively bias the silicon transistor and the compound transistor as an amplifier when the switch receives a control signal associated with an amplifier configuration.

15.(Original) The semiconductor structure of claim 11 wherein the silicon transistor comprises a gate, a first source/drain connection and a second source/drain connection coupled with the switch and the compound transistor comprises a gate, a first source/drain connection coupled with the switch and a second source/drain connection.

16.(Original) The semiconductor structure of claim 15 wherein the switch is responsive to a first control signal value for coupling the second source/drain connection of the silicon transistor and the first source drain/ connection of the compound transistor.

17.(Original) The semiconductor structure of claim 16 wherein the switch is responsive to a second control signal value for coupling the second source/drain connection

of the silicon transistor to a ground potential and for coupling the first source/drain connection of the compound transistor to an output network.

18.(Original) The semiconductor structure of claim 17 further comprising:

a matching network configured to combine an output signal from the first source/drain connection of the silicon transistor and another output signal from the first source/drain of the compound transistor at an output.

19.(Original) The semiconductor structure of claim 18 further comprising bias circuits for selectively biasing gates of the silicon transistor and the compound transistor.

20.(Original) The semiconductor structure of claim 11 wherein the switch comprises a micro-electro-mechanical system (MEMS) switch.

21.(Original) The semiconductor structure of claim 11 wherein the control circuit comprises a digital logic circuit formed at least in part in the monocrystalline silicon substrate.

22. (Currently amended) A semiconductor structure comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer; and

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline silicon substrate;~~

~~an amorphous oxide material overlying the monocrystalline silicon substrate;~~

~~a monocrystalline perovskite oxide material overlying the amorphous oxide material;~~

~~a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material~~;

one or more silicon transistors formed at least in part in the monocrystalline silicon substrate;

one or more compound transistors formed at least in part in the monocrystalline compound semiconductor material; and

switches associated with respective transistors of the one or more silicon transistors and the one or more compound transistors, the switches receiving control signals for selectively coupling the respective transistors to one of the signal input circuit and the signal output circuit.

23.(Original) The semiconductor structure of claim 22 further comprising:

a control circuit coupled with the switches to provide the control signals.

24.(Original) The semiconductor structure of claim 23 wherein the control circuit is formed at least in part in the monocrystalline silicon substrate.

25.(Original) The semiconductor structure of claim 22 further comprising a matching network configured to combine signals from two or more transistors.

26. – 36 (Cancelled)

37. (Currently Amended) A semiconductor structure comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer; and

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline silicon substrate;~~

~~an amorphous oxide material overlying the monocrystalline silicon substrate;~~

~~a monocrystalline perovskite oxide material overlying the amorphous oxide material;~~ ~~and~~

~~a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material~~;

at least one configurable transistor formed at least in part in the monocrystalline compound semiconductor material; and

a control circuit electrically coupled with the transistor and formed at least in part in a silicon portion of the semiconductor structure.

38.(Original) The semiconductor structure of claim 37 further comprising:

at least one silicon transistor electrically coupled with the control circuit and formed at least in part in the silicon portion of the semiconductor structure.

39.(Original) The semiconductor structure of claim 37 wherein the at least one configurable transistor is configurable in response to a signal received from the control circuit.

40. – 48. (Cancelled)